

# Stress Test Integrated Circuits (ICs) with a Function Generator

Approach and techniques for conducting stress tests on IC with function generators

# Integrated Circuits (ICs) Stress Testing

Stress testing is a rigorous reliability assessment methodology used to evaluate an Integrated Circuit's (IC) performance under extreme or accelerated conditions. This critical process identifies potential failure modes that may not manifest during typical operation but could emerge over the long term or in harsh environmental conditions. By intentionally pushing an IC beyond its specified operating parameters, these tests effectively reveal weaknesses in design, manufacturing, or materials.

This application note focuses on utilizing a function generator as the primary instrument for generating precise electrical signals to simulate various operating conditions and induce these critical stresses. When paired with an oscilloscope for observation and a DC power supply for baseline power, a function generator facilitates cost-effective and insightful stress testing through its ability to provide a wide range of non-ideal signals and modulations. The overarching objective is to thoroughly evaluate an IC's robustness, characterize its performance boundaries, and identify failure mechanisms under conditions exceeding its typical operating specifications.

## Stress testing IC using function generators

Function generators play a crucial role in this process by enabling the simulation of diverse stress conditions, including:

- **Voltage stress:** Applying dynamic voltage changes, such as overvoltage, undervoltage, and voltage transients, to assess the IC's robustness against power rail fluctuations and surges.
- **Frequency stress:** Introducing frequency sweeping using relevant waveforms (e.g., square waves for digital clocks, sine waves for analog inputs) to observe output signal degradation, thereby revealing bandwidth or speed limitations.
- **Slew rate (rise/fall time) stress:** Precisely controlling the rise and fall time capabilities of pulse or square wave outputs to identify false triggering, oscillations, or increased propagation delays associated with non-ideal signal edges.
- **Noise injection:** Introducing controlled noise (e.g., white noise, periodic noise) into signal paths to rigorously assess the IC's immunity to various forms of electrical interference.

The specific stress tests will vary depending on the type and function of the IC. The function generator's outputs can be tailored to stress the sensitivity of each IC type:

IC type	Devices Under Test (DUT)	What is the function generator's role in this?
Digital	Microcontrollers, logic gates, FPGAs, ASICs	Create a clock signal, vary input voltage levels, and modulate power supply stability.
Analog	Op-Amps, ADC/DAC, sensors	Provide varied input voltage ranges, introduce noise, sweep frequencies, and generate ripple.
Power management	DC-DC converters, LDO	Modulating input voltage and testing dynamic regulation accuracy
Communication	Transceivers, RF IC	Simulate signal integrity issues, inject noise or distortion, and sweep frequencies.

# Voltage Stress Testing

Voltage stress testing involves applying voltages beyond the normal operating range to an IC to evaluate its behavior under extreme conditions. By pushing the IC to its limits, one can identify potential areas where the IC might fail under unexpected voltage surges or determine how well the IC can withstand voltage fluctuations and transients. This process yields valuable insights into the IC's robustness and reliability.

Function generators are essential tools in voltage stress testing due to their ability to produce a variety of electrical signals with precise control over parameters like amplitude, frequency, and waveform shape. This flexibility allows us to simulate various real-world scenarios and abnormal operating conditions that the IC might encounter.

The table below summarizes the common voltage stress types and their associated waveform requirements generated by the function generator, including:

Stress test	Purposes	To evaluate on	Observation	Function generator configuration
Over-Voltage	Test IC tolerance to voltages above its maximum rating.	Robustness against accidental overvoltage events	Monitor for junction breakdown, dielectric breakdown, or electromigration, which are standard failure modes.	Output a DC voltage or a ramp waveform. Amplitude should be set to exceed the IC's maximum specified voltage.
Under-Voltage	Assess IC behavior below the minimum operating voltage.	Performance during brown-out conditions or power supply drop	Look for supply voltage brownout, reset failures, or data corruption.	Output a DC voltage or a ramp waveform. The amplitude should be set to fall below the IC's minimum specified operating voltage.
Voltage Transients	Simulate sudden voltage spikes or drops to test the IC's robustness to these rapid changes.	Immunity to power line disturbances or inductive switching events	Check for latch-up, logic errors, or data corruption.	Generate square or pulse waveforms. The amplitude will typically be nominal, but with a significant voltage swing (10% to 30% of nominal voltage). Pulse widths are usually narrow (1-100 $\mu$ s).
Power Cycling / Ripple	Mimic power supply fluctuations and assess stability.	How well the IC maintains performance under varying power supply conditions	Check for capacitor failure, electromigration, or degradation of power supply components.	Output a sine or triangle waveform. The amplitude should be a percentage of the nominal voltage (5-10% of nominal). Frequencies typically range from 50 Hz to 100 kHz.

To carry out a voltage stress test effectively, several key parameters need to be considered for performance evaluation:

Key parameters	Definition
Stress type	Clearly define the specific voltage stress being applied.
Voltage level / Amplitude	Set the precise voltage level or amplitude based on the type of stress and test objective.
Duration	Define the time the IC is exposed to the stress voltage, ranging from seconds to hours, depending on the test objective.
Monitoring	Continuously observe the current consumption, signal integrity, and temperature to detect the onset of failure.
Pass / fail criteria	Defined thresholds for acceptable variations in performance metrics

## Frequency Stress

Frequency stress testing evaluates an IC's performance and stability when operating at frequencies outside its specified range. This is particularly critical for digital ICs that rely on precise clock signals and analog ICs where bandwidth and frequency response are key performance indicators. By pushing the IC to its frequency limits, engineers can identify operational margins, potential timing violations, and signal degradation. Two common types of frequency stress types will be discussed using a function generator:

### Frequency margining

Frequency margining is a stress test used to evaluate an IC's performance and stability by operating it outside its specified frequency range. This test is critical for both digital ICs, which depend on precise clock signals, and analog ICs, where bandwidth and frequency response are key. By intentionally exceeding the IC's frequency limits, both above and below the specified range, engineers can identify operational margins, potential timing issues, and signal degradation. This process helps to validate the design, characterize the IC's true capabilities, and ensure it will function reliably in real-world conditions where component variations and environmental factors can affect performance. A function generator is an ideal tool for this test because it can produce a wide range of waveforms and sweep through frequencies, allowing for a controlled exploration of the IC's boundaries.

To perform a frequency margining test, use a function generator to stress the IC with controlled frequency sweeps. This test identifies the minimum and maximum operational frequencies for the IC.

After the initial setup, the test has two parts:

- **Over-frequency margining:** Use the function generator's sweep function to increase the frequency from the nominal value automatically. Monitor the IC's output and note the frequency at which it fails. This is the maximum operational frequency.
- **Under-frequency margining:** Reset the generator and sweep the frequency down from the nominal value. The frequency at which the IC fails is its minimum operational frequency.



**Figure 1.** Performing over-frequency margining on Channel 1 and under-frequency margining on Channel 2 with the FG33532A function generator.

## What to observe?

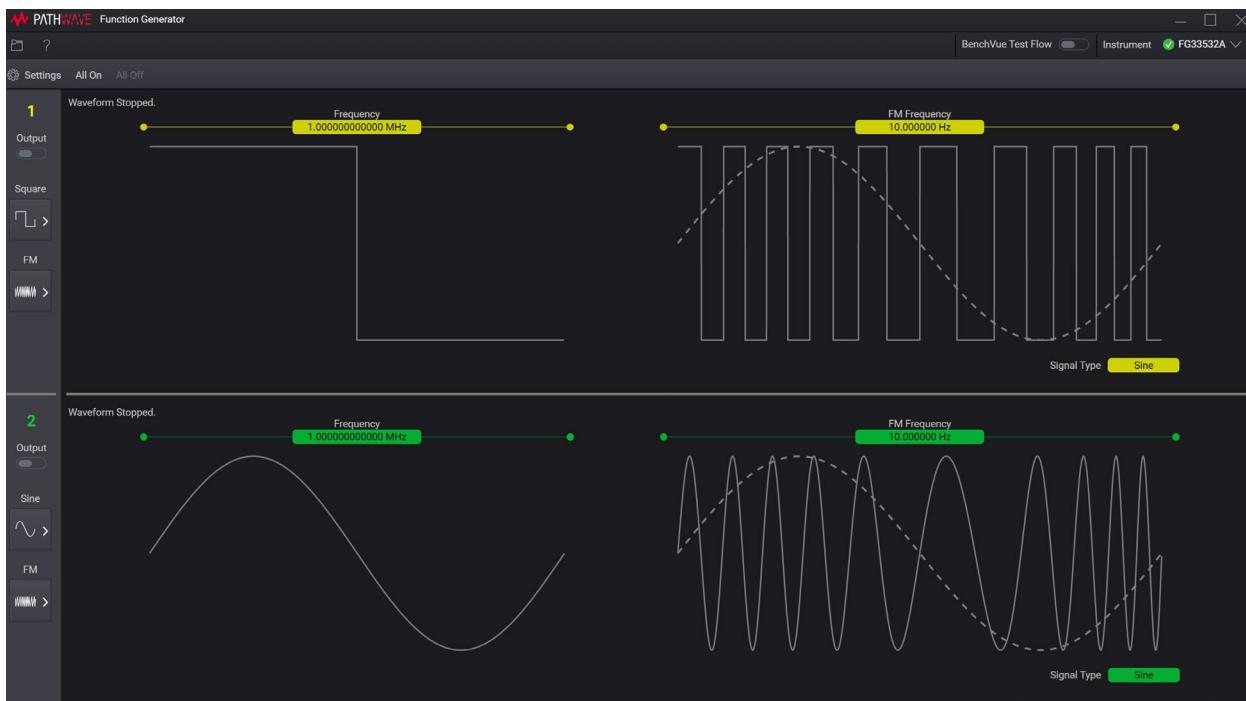
During the test, observe the IC's output for signs of failure, such as amplitude drop-off or increased distortion in analog ICs. For digital ICs, look for incorrect logic states, unstable outputs, or timing violations, such as increased propagation delays. The frequencies at which these issues occur define the IC's true operating range, ensuring your system design has an adequate margin for reliable performance.

## Frequency Modulation (FM) stress

FM stress testing is critical for applications where input signals are not static, such as in communication systems or control loops, and helps identify an IC's ability to track frequency changes without signal degradation or functional errors. It is a method for evaluating how an IC responds to dynamic changes in its input signal frequency. Unlike frequency margining, which tests static frequency limits, FM stress introduces continuous, controlled frequency variations that simulate real-world modulated signals. This is particularly relevant for communication ICs, such as transceivers, and systems that process signals with inherent frequency variations. By subjecting an IC to this test, engineers can assess its dynamic frequency response, tracking accuracy, and stability under non-ideal, time-varying conditions. A function generator with FM capabilities is the core instrument for this test, as it provides precise control over the modulation parameters.

To perform this test, configure the function generator to produce an FM waveform by setting carrier frequency ( $f_c$ ) to the IC's nominal operating frequency and then adjusting the modulation

frequency (fm) and the frequency deviation ( $\Delta f$ ), which is the amount by which the carrier frequency will vary from its nominal value and then gradually increase the frequency deviation and the modulation frequency while carefully observing the IC's output on the oscilloscope.



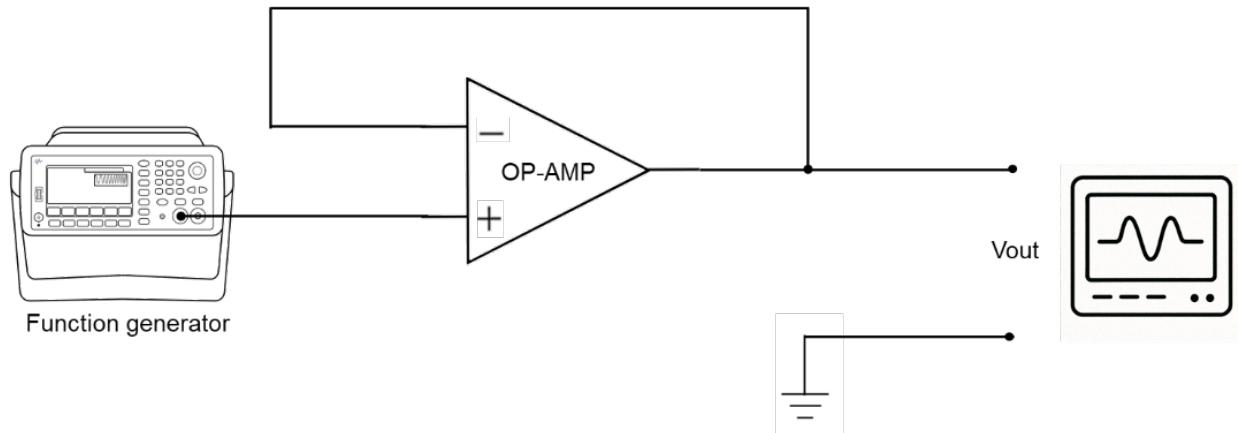
**Figure 2.** Generate a square wave with FM on Channel 1 and a sine wave with FM on Channel 2 using the FG33532A function generator and Pathwave Function Generator application.

## What to observe?

During observation and interpretation, look for several key indicators of performance degradation. This includes tracking errors, where the IC's output signal may fail to track the frequency changes of the input signal. You might also see signal distortion, where the output waveform shows increased distortion or noise as the modulation parameters increase. At extreme modulation, a loss of function can occur, causing the IC to stop working, lose synchronization, or produce incorrect data. An increasing phase shift between the input and output signals can also indicate a limitation in the IC's high-frequency response.

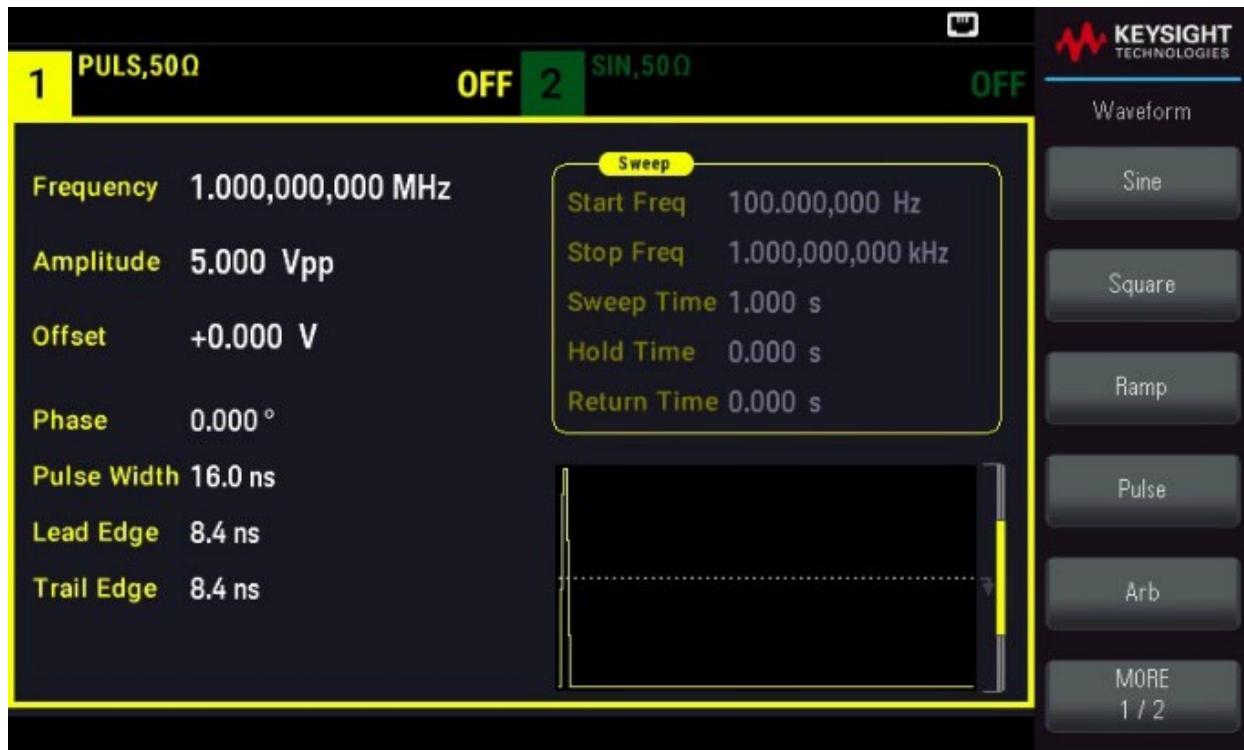
# Slew Rate (Rise / Fall Time) Stress

Slew rate stress testing is essential for verifying an IC's ability to operate correctly with slow or fast signal edges, which can lead to issues such as false triggering, increased propagation delays, and oscillation. A function generator with precise control over pulse width, duty cycle, and most critically, rise and fall times, is the ideal tool for this analysis.

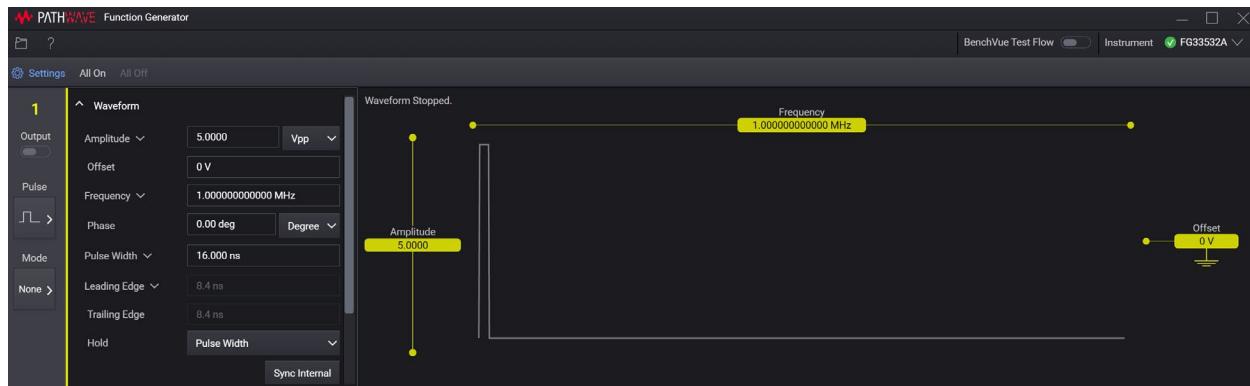


**Figure 3.** Test setup block diagram of slew rate stress.

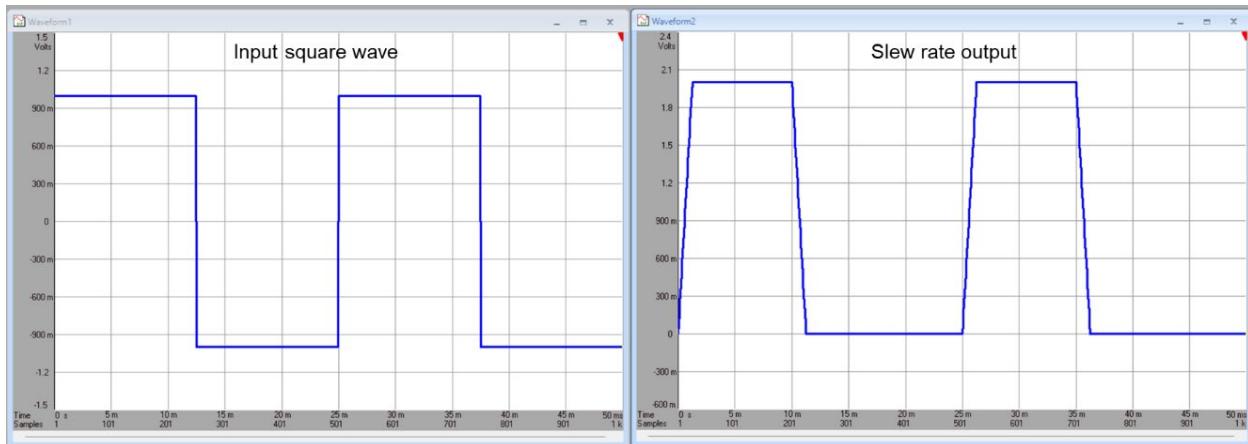
Slew rate is defined as the range of change of a signal's voltage over time ( $dV/dt$ ). It is a critical parameter for both digital and analog circuits. For digital ICs, the rise and fall times of a clock or data signal can significantly impact timing. An input signal with a rise time that is too slow may lead to false triggering or oscillations as the IC's input stages spend more time in an ambiguous voltage region. Conversely, an excessively fast rise time can cause signal integrity issues such as overshoot, undershoot, and ringing, which can also stress the input circuitry. Slew rate stress testing addresses these concerns by intentionally pushing the IC's input pins with a range of rise and fall times. The objective is to identify the maximum and minimum slew rates at which the IC still operates within its specified performance envelope. A function generator with Arbitrary Waveform Generation (AWG) or pulse generation capabilities is essential for this, as it allows for independent and precise control over the rise and fall times of the output signal.



**Figure 4.** FG33532A function generator setting screen with the smallest possible rise and fall time of 8.4 ns.



**Figure 5.** Function generator setting using the Pathwave BenchVue Function Generator application



**Figure 6.** Input square wave from the function generator compared to the output waveform from the op-amp, limited by the slew rate.

The function generator plays a pivotal role in this test procedure. Begin by establishing a baseline by generating a pulse wave with a fast, sharp edge well within the IC's specified limits. For Slow slew rate stress, gradually increase the rise and fall times on the function generator, often using a dedicated menu or sweep function. As the edges slow down, monitor the IC's output to find the slowest slew rate at which it still functions correctly, observe for increased propagation delay, false triggering, or functional errors. For fast slew rate stress, decrease the rise and fall times to the fastest rate the generator can produce, and look out for output issues like overshoot and undershoot that indicate a drive strength problem. By using the function generator to vary these parameters systematically, you can effectively identify the IC's slew rate limits.

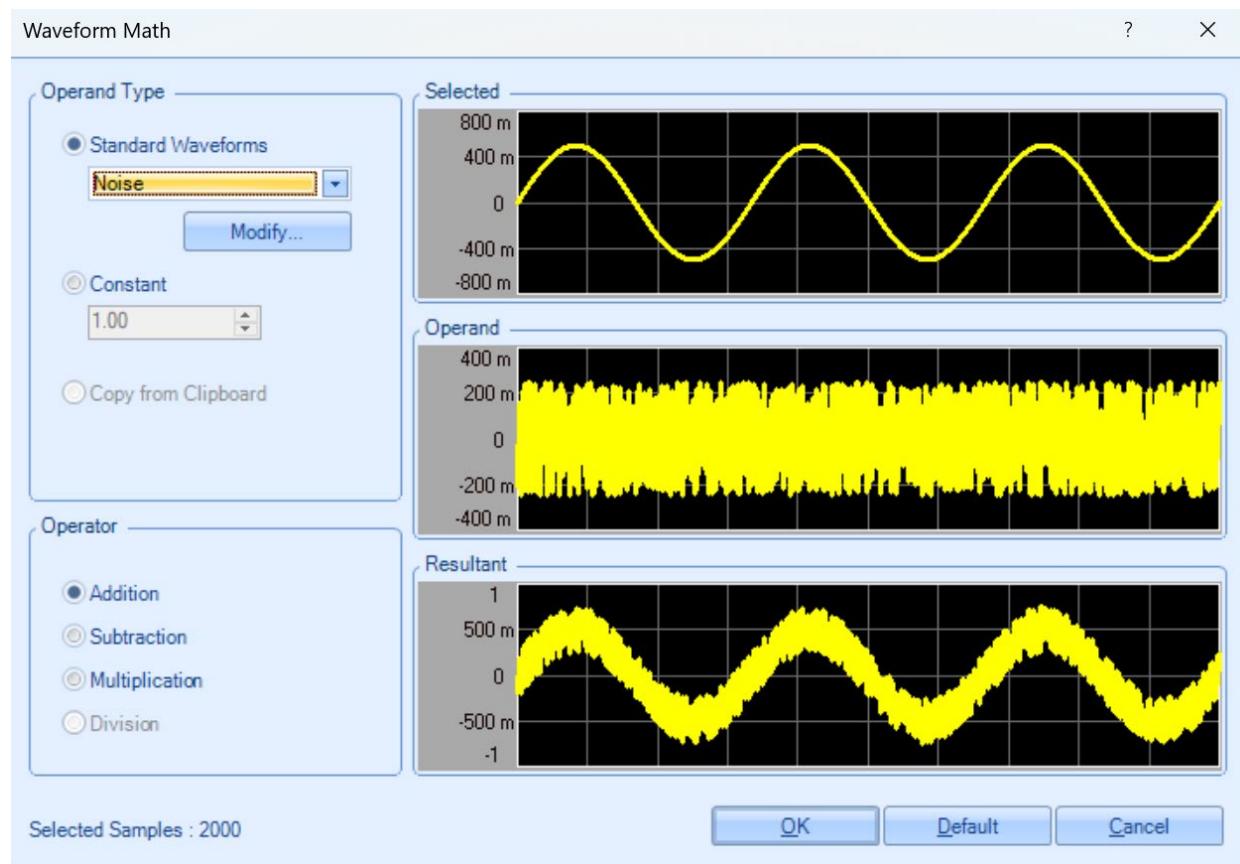
## Noise Susceptibility Test and Noise Superposition

Noise susceptibility testing is crucial for evaluating how well ICs function in the presence of external noise and electromagnetic interference (EMI). This test ensures reliable operation in real-world environments where noise from power supplies, crosstalk, and electromagnetic waves is common. The goal is to meet performance targets and comply with industry standards like IEC 61000-4 (EMC).

This testing is particularly critical for applications such as automotive systems, consumer electronics, and industrial equipment, where external noise sources are abundant. For instance, microcontrollers and microprocessors, often considered the "brains" of electronic systems, are susceptible to noise. External disturbances can cause these devices to malfunction or crash, leading to system errors. Similarly, sensors (e.g., temperature, pressure, accelerometers) that convert physical signals into electrical outputs are vulnerable to noise. Noise can distort these signals, resulting in inaccurate readings or system failures. In industrial or medical applications, for example, corrupted sensor outputs due to noise could lead to performance degradation or hazardous conditions.

Noise susceptibility testing can be effectively conducted using a function generator to simulate representative noise waveforms. The testing regimen typically includes noise superposition on standard and arbitrary waveforms, as well as pulse injection. To simulate noise coupled onto the signal path, configure the function generator to add random or periodic noise to a standard input signal. This process is known as noise superposition. Furthermore, the function generator's pulse capabilities can inject narrow, high-amplitude pulses directly onto the signal, thereby creating signal corruption.

The IC's robustness will be evaluated based on performance metrics such as Signal-to-Noise Ratio (SNR) and error rates (for digital ICs). An elevated SNR and reduced error rates indicate superior signal integrity and enhanced reliability of communication and data transmission in the presence of the function generator's injected noise. During testing, monitor for incorrect logic states, data corruption, analog signal distortion, or complete system malfunction.



**Figure 7.** Adding noise to the sine wave using the addition operator using the BenchLink Waveform Builder Pro app.

# Conclusion

Function generators serve as critical tools for generating signal stimuli during comprehensive IC characterization. They are used to stress test devices by simulating harsh operating conditions, such as voltage and frequency extremes. Furthermore, these instruments provide the necessary waveforms to precisely evaluate performance and control switching transitions, particularly double pulse testing. Ultimately, the ability to validate IC behavior under a wide range of operational parameters is essential for ensuring the reliability and efficiency of electronic systems.

## For more information

To learn more about Keysight's offering for function generators, go to [Waveform and Function Generators](#)

Keysight enables innovators to push the boundaries of engineering by quickly solving design, emulation, and test challenges to create the best product experiences. Start your innovation journey at [www.keysight.com](http://www.keysight.com).